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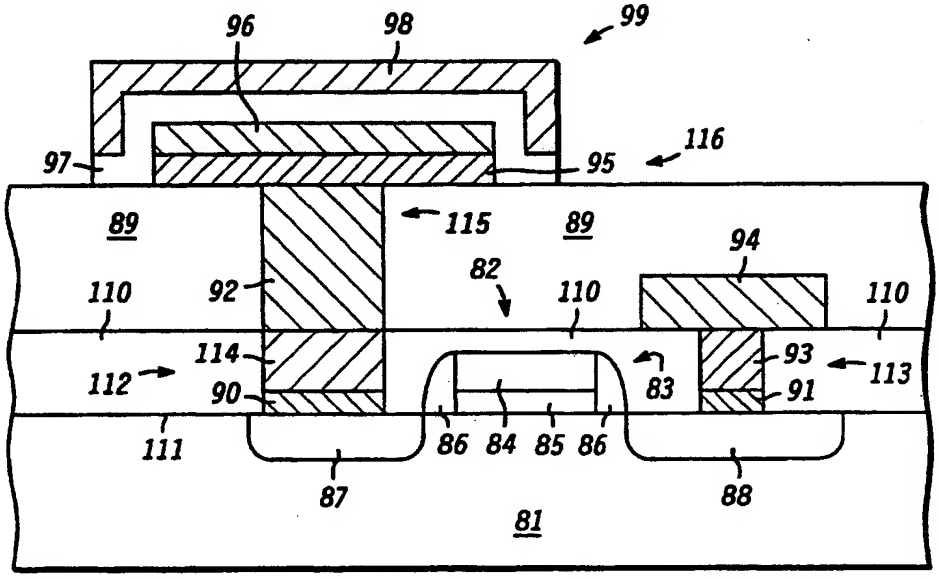

(57) Abstract

A semiconductor device (80) includes a transistor (82) and a capacitor structure (99, 120). The capacitive structure (99, 120) includes a dielectric material (97) between two conductive plates (98, 116). The transistor (82) has current carrying electrodes (87, 88), one of which is connected to the capacitive structure (99, 120) with a plug (92).

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SEMICONDUCTOR DEVICE WITH FERROELECTRIC CAPACITOR DIELECTRIC AND METHOD FOR MAKING

Background of the Invention

This invention relates, in general, to electronic components, and more particularly, to dielectric materials used in the manufacture of electronic components.

Dielectric materials such as silicon dioxide and silicon nitride are used in a variety of applications including use as the insulating material between two conductive plates in a capacitor structure. The effective capacitance value of a given capacitor is determined in part by the dielectric constant of the dielectric material and the area of the dielectric material between the two plates. In order to decrease the relative size of the capacitor and yet form a capacitor having the same capacitance value, there has to be a proportional increase in the dielectric constant of the material used in the capacitor.

Currently, conventional dielectric materials suffer from one of four problems: they are incompatible with the materials used to form electronic components; they do not have a high enough dielectric constant; they have a Curie temperature within the operational range of the electronic component; or they have high leakage current densities.

Accordingly, it would be advantageous to provide a dielectric material that can be used in the manufacture of electronic components that has a higher dielectric constant value and lower leakage current densities. It would also be advantageous if the dielectric material had a Curie temperature that was below the operational temperature of electronic component so the dielectric material does not change from a paraelectric state to a ferroelectric state during normal operation of the electronic component.

Brief Description of the Drawings

FIG. 1 illustrates enlarged cross-sectional views of electronic components formed in accordance with the present invention;

FIG. 2 is cross-sectional view of a sputtering deposition system; and

FIGs. 3-6 illustrate enlarged cross-sectional views of semiconductor devices formed in accordance with the present invention.

It will be appreciated that for simplicity and clarity of illustration, elements illustrated in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements are exaggerated relative to other elements for clarity. Further, where considered appropriate, reference numerals have been repeated among the figures to indicate corresponding or analogous elements.

Detailed Description of the Drawings

In general, the present invention provides a novel dielectric material that can be used in the manufacture of electronic components in a variety of applications. More particularly, the present invention provides examples of how this dielectric material can be used in capacitor structures as the charge storage device for dynamic random access memories (DRAMs) or embedded DRAM structures in either capacitor-over-bit line (COB) or capacitor-under-bit line (CUB) structures.

However, one skilled in the art will appreciate that the present invention can be used to manufacture integrated circuits such as microprocessors, microcontrollers, sensors, embedded DRAMs, static random access memories (SRAMs), an electrically erasable and programmable read only memory (EEPROM), a flash electrically programmable read only memory (flash EPROM), or a flash electrically erasable and programmable read only memory (flash EEPROM). In addition, the dielectric material of the present invention can also be used to form discrete components such as stand-alone capacitors.

Due to the insulating properties of the dielectric material, the present invention can be used to replace conventional dielectric materials. In the examples discussed below, the dielectric material of the present invention can be used to replace silicon dioxide or silicon nitride as the insulating material in a gate structure, a capacitor structure, or a non-volatile memory device.

The dielectric material of the preferred embodiment comprises barium, titanium, tin, and an oxide. More particularly, the dielectric material can be represented by the formula:

$$Ba(Ti_{(1-x)}\ Sn_x)O_3.$$

Where X can range from a value greater than zero to about 1. This formula is intended to represent the solid solution form of the dielectric material of the present invention. It should be noted that the solid solution formula differs from a dielectric material that is lightly doped with either barium, titanium, or tin, because each of the elements in the formula (Ba, Ti, Sn, and O) is intended to be a major constituent of the compound. As one skilled in the art will appreciate, this is more than just impurity concentration levels.

One unexpected property of the dielectric material of the present invention is that the addition of Sn to a compound provides a material that is classified as a dielectric material. This is in contrast to what might be more commonly expected; a conductive material such as is used in the formation of interconnect structures or leadframes. Instead, the addition of tin to the compound of the present invention provides a material that has a dielectric constant greater than 1 and a resistivity greater than 1×10^5 ohm-centimeters. Historically, a dielectric constant greater than 1 has been the value used by those skilled in the art to classify a material as a dielectric material rather than a conductive or merely resistive material. Functionally, the material of the present invention is well suited for applications where the material is used to provide electrical isolation between conductive structures, and yet, provide capacitive coupling between the conductive structures. For example, if the dielectric material is placed between two conductive regions or plates, the dielectric material will retard the flow of current between the plates and allow the conductive plates to be capacitively coupled together.

Another unexpected property of the dielectric material is that the relative value of the concentration of tin in the compound can be varied to adjust the Curie temperature of the compound. In particular, the value of X in the formula shown above can be varied to provide a

compound having a different Curie temperature. The Curie temperature of a material is the temperature at which the material changes from being paraelectric to ferroelectric or vice versa. A paraelectric material is said to have a single polarization value at the voltage potential applied. A ferroelectric material, however, exhibits a hysteresis in polarization which depends on the previous and present voltage potential applied to the material.

In most applications, it is desirable to form a dielectric material that remains paraelectric in nature. This allows an electronic component to be formed that has a predictable and consistent polarization. To maintain the paraelectric property of the dielectric material, the Curie temperature of the material must be below the normal operating temperatures of the electronic component so that the dielectric material does not pass through its Curie point. For example, if an electronic component is normally operated at about 0° Celsius (C) to 100°C, then ideally, the Curie temperature of the material should be -25°C or lower.

In addition to changing its electrical characteristics as described above, a dielectric material also undergoes significant physical stress as it passes through its Curie temperature. Therefore, it is desirable to form the dielectric material so that its Curie temperature is outside of its normal operating temperature range. This prevents the dielectric material, and the electronic component containing the dielectric material, from being damaged during operation because the dielectric material does not transform from the paraelectric state to the ferroelectric state.

One skilled in the art, however, will appreciate that there are some applications where it is desirable to form an electronic component having a dielectric material that is ferroelectric in nature. For example, it may be desirable to form a non-volatile memory cell using a ferroelectric dielectric material and use the two polarization states to represent the programmed and erased states of the non-volatile memory cell.

FIG. 1 illustrates enlarged cross-sectional views of examples of applications in which the dielectric material of the present invention can be used. For example, the dielectric material can be used to form a

capacitor structure as shown in electronic components 40 and 50. Electronic component 40 is a capacitor that is formed on a substrate 41. Substrate 41 is preferably a semiconductor substrate, however, other substrate materials used by those skilled in the art can also be used. Electronic component 40 has a layer of dielectric material 43, hereinafter referred to as dielectric layer 43, sandwiched between conductive plates 42 and 44.

In this embodiment, dielectric layer 43 is preferably paraelectric so that electronic component 40 has a predictable and constant polarization value. Accordingly, the relative amount of tin in the $Ba(Ti_{(1-x)}\ Sn_x)O_3$ compound should be adjusted so that the Curie temperature of dielectric layer 43 is less than the normal operating temperature of electronic component 40. For example, a value of x ranging from about 0.15 to 0.3 provides a dielectric material that has a Curie temperature ranging from about -25°C to -100°C. Therefore, as long as electronic component 40 remains above -25°C, dielectric layer 43 remains paraelectric.

Table 1 below provides other ranges for the value of X in the compound $Ba(Ti_{(1-x)}\ Sn_x)O_3$ producing a dielectric material having various Curie temperatures. Table 1 also lists the property of the material at 0°C and -25°C, respectively. The value of '>0' is used to indicate a concentration greater than zero and can have a value of 0.001, 0.0001, 0.00001, or less depending on the measurement capability. The value of '<1' is used to indicate a concentration less than 1 and can have a value of 0.99, 0.999, 0.9999, or greater depending on the measurement capability.

TABLE 1

Value of X	Curie Temperature	0°C Property	-25°C Property
>0 to 0.1	120°C to 40°C	ferroelectric	ferroelectric
0.1 to 0.3	40°C to -125°C	either	either
0.15 to 0.3	0°C to -125°C	either	either
0.18 to 0.3	-25°C to -125°C	paraelectric	either
0.01 to 0.1	119°C to 40°C	ferroelectric	ferroelectric
0.01 to 0.3	119°C to -125°C	either	either
>0 to <1	less than 120°C	either	either

As shown in the examples provided in Table 1, it is possible to form a dielectric material that is paraelectric at a temperature of about 0°C or is ferroelectric at a temperature of about 0°C. It is also possible to form a dielectric material that has a Curie temperature less than 0°C or that has a Curie temperature less than -25°C. It is also possible to form a compound where x ranges from about 0.2 to 0.4, about 0.3 to 0.5, about 0.4 to 0.6, about 0.5 to 0.7, about 0.6 to 0.8, about 0.7 to 0.9, about 0.8 to 1, and 0.9 to 1.

In the preferred embodiment, dielectric material 43 comprises the compound $Ba(Ti_{(1-x)}\ Sn_x)O_3$, which results in a dielectric material having a bulk dielectric constant ranging from about 28,000 to 35,000. This is certainly greater than about 1 and is greater than about 10, which is larger than the dielectric constants of silicon dioxide and silicon nitride. The dielectric constant of the material of the present invention is also greater than about 300, which exceeds the thin film dielectric constant of barium-strontium-titanium-oxide. This corresponds to a bulk dielectric constant for barium-strontium-titanium-oxide of about 15,000 to 20,000.

As shown in Table 1, a compound has been provided that includes tin, yet provides a dielectric material. It may also be possible to form other compounds that include tin, or tin and titanium, that provides a material having dielectric characteristics. In addition, the compound of the preferred embodiment includes oxygen, but it should be understood that other oxides can also be used.

As shown in FIG. 1, electronic component 40 includes conductive plates 42 and 44 that are in direct contact with dielectric material 43. It should be understood that it is not necessary for dielectric material 43 to be in direct contact with conductive plates 42 and 44 as other dielectric materials such as silicon nitride, silicon dioxide, or silicon oxy-nitride can be formed therebetween. Additionally, the lower conductive plate of the capacitor structure can be replaced with a doped region 52 formed in substrate 41 as illustrated in electronic component 50. Therefore, the dielectric material of the present invention can be placed between two conductive regions to provide a capacitor structure.

The dielectric material of the present invention can also be used to form an electronic component 60 such as a non-volatile memory cell. For example, dielectric layers 61 and 63 comprising $Ba(Ti_{(1-x)}\ Sn_x)O_3$ can be used to electrically isolate a floating gate 62 from an underlying channel region 67 in substrate 41 and to electrically isolate floating gate 62 from a control gate 64. Channel region 67 refers to the portion of substrate 41 between a source region 65 and a drain region 66. It should be understood that dielectric layers 61 and 63 need not solely be formed using the dielectric material of the present invention and that it is not necessary that both layers comprise $Ba(Ti_{(1-x)}\ Sn_x)O_3$. It is also possible to include other dielectric materials such as silicon dioxide, silicon nitride, or the like in each of dielectric layers 61 and 63. Preferably, the dielectric material of the present invention is ferroelectric when used in a non-volatile memory. Thus, x can have a value ranging from about 0.01 to 0.1 or from about 0.05 to 0.1.

Also shown in FIG. 1 is an electronic component 70 that illustrates how the dielectric material of the present invention can be used as a gate dielectric material. Electronic component 70 has a layer of dielectric material 71 between a gate structure 72 and substrate 41 that is used to electrically isolate gate structure 72 from a channel region 75. In the operation of electronic component 70, a voltage potential is placed on gate structure 72 to modulate channel region 75 between a source region 73 and a drain region 74.

Methods of forming an electronic component having a dielectric material comprising tin in accordance with the present invention are now provided. One method of forming dielectric materials 43, 61, 63, or 71 is to use a metal organic decomposition process or a solution-gelation (sol-gel) process. For example, a solution is prepared containing precursors of the desired elements in the proper ratios. The solution is then dispensed or spun over the surface of a substrate to form a layer of the solution across the substrate. The solution is then heated or annealed to drive off the organic materials in the solution, thereby forming a layer of dielectric material having the desired composition.

A source of tin can be added to the solution using a precursor such as tin beta-n-butoxide, tin chloride, tin acetate, tin nitrate, tin lactate, tin ammonium acetate, tin tetra-isopropoxide, or tin

isopropoxide. A source of titanium can be added to the solution using a precursor such as titanium tetra-n-butoxide, titanium di-tertiary-butoxyl-tetramethyl heptanodionate, titanium tetra-tertiary butoxide, titanium ditetramethyl-heptano-dionate disopropoxide, titanium tetraethoxide, titanium lactate, titanium ammonium acetate, titanium tetra-isopropoxide, or titanium isopropoxide. A source of barium can be added to the solution using a precursor such as beta-diketonate complexes of barium tetramethylheptanodionate, barium hexaflouroacetylacetonate, barium(2,2,6,6-tetramethyl-3,5-heptanedione)$_2$, barium hexaflouroacetylacetone, or barium tetrafluoroacetylacetone.

It is also possible to form a layer of dielectric material in accordance with the present invention using an ion sputtering or reactive ion sputtering (RIS) process such as is illustrated in FIG. 2. FIG. 2 illustrates a cross-sectional portion of a radio frequency (RF) sputtering system 10. It should also be understood that the present invention can also be used in a Direct Current (DC) sputtering system and one skilled in the art will understand the appropriate modifications that are required. System 10 includes a sputtering chamber 11 in which the RF sputtering occurs. A sputtering target 12 is utilized as a source of material for forming a film 16 such as a dielectric layer on a surface of a semiconductor substrate 13, which is placed on an heating element 14. Material is transferred from sputtering target 12 to film 16 by RF sputtering. An RF voltage source 15 is coupled to target 12 and to substrate 13 to facilitate the RF sputtering operation.

Sputtering target 12 comprises the desired amounts of barium, titanium, and tin and can be formed by mixing barium oxide, titanium oxide, and tin oxide in the correct proportions to form a ceramic sputtering target. Subsequent to mixing, pressure and temperature are utilized to transform the mixture into sputtering target 12. For example, the mixture can be cold pressed at a pressure of about three hundred atmospheres (atm), and then sintered at a temperature of approximately 1200° C at atmospheric pressure. These pressures and temperatures can vary depending on furnace and target sizes and also on target composition.

Thereafter, target 12 is placed in sputtering chamber 11 along with substrate 13. Target 12 and substrate 13 are connected to RF voltage source 15 in order to provide an electric field and facilitate sputtering material from target 12 onto the surface of substrate 13. Typically, voltage source 15 applies approximately five hundred volts to target 12 and substrate 13. A plasma is formed using an argon-oxygen or oxygen ambient within chamber 11 in order to complete the RF sputtering. RF sputtering operations are well known to those skilled in the art.

It is also possible to form dielectric layer 16 using a sputtering target made from barium oxide, tin oxide, and titanium powder. The sputtering target and substrate 13 are placed into sputtering chamber 11, which is filled with an ambient containing oxygen. As portions of the sputtering target are transferred to substrate 13 using a DC sputtering process, oxygen is incorporated in the desired proportion to form a dielectric material. It is also possible to anneal or heat the substrate in an oxygen-rich ambient after dielectric layer 16 is deposited instead of sputtering in an oxygen rich ambient.

It is also possible to form the dielectric material of the present invention using a metallorganic chemical vapor deposition (MOCVD) process. In such a process, some of the precursors listed earlier are transported to a reaction chamber using a carrier gas in the desired proportions. The reaction conditions depend in part on the precursors selected and will be understood by those skilled in the art.

Turning now to FIG. 3, a more detailed description is provided of how the dielectric material of the present invention can be used to form a semiconductor device 80 such as a dynamic random access memory. To begin, a transistor 82 is formed on a substrate 81 using conventional techniques. Preferably, transistor 82 is a field effect transistor (FET) that has current carrying electrodes 87 and 88 formed in semiconductor substrate 81. Current carrying electrodes 87-88 can be the source and drain regions of transistor 82. Preferably, transistor 82 has a gate structure 83 that is used to control a current flow between current carrying electrodes 87 and 88. Gate structure 83, for example, can have a conductive layer 84 that is capacitively coupled to semiconductor substrate 81 by a gate oxide layer 85. Gate structure 83 can also have

sidewall spacers 86 that can be optionally formed to electrically isolate conductive layer 84 from neighboring structures (not shown).

An insulating layer 110 is then deposited over transistor 82 and a surface 111 of substrate 81. Preferably, a layer of silicon dioxide or phosphosilicate glass is deposited using either a chemical vapor deposition process (CVD) or a plasma enhanced chemical vapor deposition (PECVD) process. The thickness of insulating layer 110 can vary as necessary and can range for example from about 300 angstroms (Å) to 5,000 Å. A chemical mechanical polish (CMP) process is then used to planarize the top surface of insulating layer 110. Thereafter, a conventional photolithographic masking and etch process is used to form openings 112 and 113 that expose portions of current carrying electrodes 87 and 88, respectively.

A conductive material such as tungsten, titanium silicide, titanium nitride, polysilicon, or amorphous silicon is formed in openings 112 and 113 to form plugs 93 and 114. Optionally, it may be desirable to form a layer of titanium silicide 90 and 91 over the exposed portions of current carrying electrodes 87 and 88 before forming plugs 93 and 114. The layers of titanium silicide 90 and 91 can improve the electrical connection between plugs 93 and 114 and current carrying electrodes 87 and 88 and retard the formation of an oxide layer on current carrying electrodes 87 and 88. If formed, layers of titanium silicide 90 and 91 can have a thickness of about 50 Å to 500 Å.

After plugs 93 and 114 are formed, a bit line 94 is formed from a conductive material such as aluminum or the like. Bit line 94 is formed using conventional deposition and etch techniques. Once formed, bit line 94 is connected to current carrying electrode 88 via plug 93. Thereafter, an insulating layer 89 is formed over bit line 94, plug 114, and insulating layer 110. Insulating layer 89 is preferably a layer of silicon dioxide that is about 300 Å to 5,000 Å thick. Depending on the thickness and planarization of insulating layer, a CMP process can be used after insulating layer 89 is formed to provide a sufficiently planar surface to allow further processing.

An opening 115 is formed in insulating layer 89 so that at least a portion of plug 114 is exposed. A plug 92 is formed in opening 115 using a material that is compatible with plug 114 such as one of the

materials listed above. The combination of plug 92, plug 114, and perhaps layer of titanium silicide 90 provides an electrical connection between current carrying electrode 87 of transistor 82 and a capacitor structure 99 that is subsequently formed over transistor 82 as explained below.

In general, capacitor structure 99 includes a layer of dielectric material 97 that is formed between an upper conductive plate 98 and a lower conductive plate 116. In the embodiment shown in FIG. 3, conductive plate 116 is made from two layers, namely, a layer of platinum 96 on a layer of titanium nitride 95. However, it should be understood that other materials may be desirable depending on the composition of plug 92 and the necessary electrical characteristics of plate 116. It is also possible to form conductive plate 116 from a single layer or a plurality of layers. For example, conductive plate 116 can be made from a single layer of platinum, a single layer of iridium, a layer of platinum on a layer of iridium on a layer of titanium nitride, a layer of iridium oxide on a layer of iridium, a layer of iridium oxide on a layer of iridium on a layer of titanium nitride, a layer of ruthenium oxide on a layer of ruthenium, a layer of ruthenium oxide on a layer of iridium oxide, a layer of platinum doped with tin, a single layer of platinum alloy, a layer of palladium on a layer of titanium nitride, or a layer of strontium-ruthenium oxide on a layer of titanium nitride.

Conductive plate 116 can be form by depositing the desired materials using a sputtering, electroplating, electron beam vaporization, CVD, or similar process. A photolithographic masking and etch process are used to pattern conductive plate 116 as shown in FIG. 3. Dielectric layer 97 is then formed on conductive plate 116 using one of the techniques described above. In a DRAM application, dielectric material 97 should be paraelectric so that the capacitance value of capacitor structure 99 is consistent during the operation of semiconductor device 80. Accordingly, dielectric layer 97 includes $Ba(Ti_{(1-x)}\ Sn_x)O_3$ and X is chosen so that dielectric layer 97 remains paraelectric over the anticipated operating temperatures of semiconductor device 80.

In most applications, X should have a value greater than about 0.1 (i.e., a concentration greater than 10 mole percent) so that dielectric

layer 97 does not become ferroelectric. More particularly, if semiconductor device 80 is to be operated between 0°C and 70°C, then X can range from about 0.15 to 0.3. Additionally, if semiconductor device 80 is to be operated between -25°C and 70°C, then X can range from about 0.18 to 0.3. As mentioned earlier, the presence of barium, titanium, and tin in the formula $Ba(Ti_{(1-x)}\ Sn_x)O_3$ is intended to indicate the solid solution formula of dielectric material 97. By having barium, titanium, and the tin in the proper proportions, a dielectric material is provided that has significantly higher dielectric constant than other materials such as barium strontium titanate (BST). The material of the present invention differs from previously known materials in that tin and titanium are used in the compound as major constituents as opposed to merely impurities.

The size and thickness of dielectric layer 97 can vary so that capacitor structure 99 has the desired capacitance value. Preferably, dielectric layer 97 has a thickness ranging from about 50 Å to 3,000 Å so that capacitor structure 99 has a capacitance density value ranging from about 10 femto-farads/micron^2 (fF/μm^2) to 60 fF/μm^2. After dielectric layer 97 is deposited, conductive plate 98 is formed by depositing a material that is compatible with the interconnect structures (not shown) that are used to provide electrical connection to capacitor structure 99 and transistor 82. For example, conductive plate 98 can be a single layer of aluminum alloy or a plurality of layers suggested above for the formation of conductive plate 116. A conventional photolithographic masking and etch process are used to pattern conductive plate 98 and dielectric layer 97 as is shown in FIG. 3.

Turning now to FIG. 4, another method of forming a capacitor structure 120 for use with semiconductor devices is provided. FIG. 4 is an enlarged cross-sectional view of capacitor structure 120 as it might be formed on insulating layer 89 so that it would be connected to the source or drain region of a transistor 82 (see FIG. 3) by plug 92. In this embodiment, the capacitive coupling between the plates of capacitor structure 120 and its dielectric material is increased by increasing the surface area of the dielectric material that is covered by the plates.

For example, the lower conductive plate of capacitor structure 120 (indicated in FIG. 4 with a bracket 127) is provided by forming in

sequence a layer of titanium silicide 121, a layer of titanium nitride 122, a layer of ruthenium 123, and a layer of ruthenium oxide 124 using conventional techniques. In this example, the layer of titanium silicide 121 is used to improve the electrical conductivity of conductive plate 127 and the layer of ruthenium oxide 124 acts as a source of oxygen to replenish oxygen vacancies that may form in dielectric layer 97. After layers 121-124 are deposited, a conventional photolithographic masking and etch process are used to pattern layers 121-124 so that conductive plate 127 has sidewalls 128.

Dielectric layer 97 is then formed using one of the methods described above so that it is in contact with the sidewalls 128 of conductive plate 127. Depending on the thickness of layers 121-124, the overall thickness of conductive plate 127 can range from about 500 Å to over 10,000 Å. The thickness of conductive plate 127 contributes significantly to the overall surface area of conductive plate 127, and thus, contributes significantly to the capacitance value of capacitor structure 120. Conductive plate 127 can have significant topography because sidewalls 128 are orthogonal to insulating layer 89. Therefore, it may be necessary to form dielectric layer 97 using the MOCVD process described above. In addition, a CVD or MOCVD process may be necessary to form conductive plate 98 so that both dielectric layer 97 and conductive plate 98 have the proper thickness over the sidewalls 128 of conductive plate 127.

Referring now to FIG. 5, an alternative method of forming capacitor structure 120 is provided that reduces the problems of forming dielectric layer 97 and conductive plate 98 along the sidewalls 128 of conductive plate 127 (see FIG. 4). The photolithographic mask and etch process can be modified such that conductive plate 127 has sidewalls 130 that are tapered. More particularly, the sputtered etch process used to pattern layers 121-124 can be directed at an angle other than orthogonal to substrate 81 (see FIG. 3) so that the sidewalls 130 of conductive plate 127 are tapered. The angle of sidewalls 130 relative to the surface 111 of substrate 81 can be varied as necessary and can range for example from about 5° to 35° off from orthogonal as shown in FIG. 4. In the embodiments shown in FIGs. 4-5, conductive plate 127 consisted of 4 layers. It should be understood that conductive plate 127 can be a single

layer or a plurality of layers as suggested above for the formation of conductive layer 116 (see FIG. 3).

Referring now to FIG. 6 an alternative method of forming capacitor structure 99 of FIG. 3 is provided. Instead of increasing the surface area of dielectric layer 97 by forming conductive plate 127 with sidewalls 128 as shown in FIG. 4, the surface area of dielectric layer 97 can be increased by forming all or part of capacitor structure 99 in a recess 137. For example, recess 137 can be formed in insulating layer 89 so that it has sidewalls 135 and a bottom surface 136 using a wet etch process, a reactive ion etch (RIE) process, or a combination of the two. Dielectric layer 97 and conductive plates 116 and 98 are then formed in recess 137 using the techniques described above. Consequently, the surface area of conductive plates 116 and 98 is increased proportionally by the length of the sidewalls 135 of recess 137.

By now it should be appreciated that the present invention provides a compound that can be used to form dielectric materials in electronic components. The present invention also provides methods of forming the dielectric material, such as by forming a sputtering target, and provides applications for its use. A dielectric layer formed in accordance with the present invention has a dielectric constant that is higher than previously known dielectric materials. As a result, an electronic component such as a DRAM can be formed in less area, yet have the same capacitance value as if the electronic component had been formed using conventional materials. Therefore, the present invention allows electronic components to be formed using less surface area, and thus, at a lower manufacturing cost.

It should also be appreciated that the present invention provides a variety of capacitor structures that employ the dielectric material of the present invention. These capacitor structures can be connected to transistors to form DRAM cells. DRAM cells formed in accordance with the present invention can have a smaller cell size than DRAMs formed using BST because the dielectric constant of the dielectric material of the present invention is higher. Accordingly, a smaller capacitor structure can be formed that has the same charge storage capability as a larger capacitor structure formed with BST.

CLAIMS

1. A semiconductor device comprising:

a substrate;

a transistor having a first current carrying electrode, wherein the first current carrying electrode is in the substrate;

an insulating layer overlying the transistor; and

a capacitor structure having a dielectric layer that is coupled to the first current carrying electrode of the transistor, wherein the capacitor structure is overlying the insulating layer, and the dielectric layer is paraelectric and comprises $Ba(Ti_{(1-x)}\ Sn_x)O_3$.

2. The semiconductor device of claim 1 wherein x is greater than about 0.1.

3. The semiconductor device of claim 1 wherein x ranges from about 0.15 to 0.3.

4. The semiconductor device of claim 1 wherein the capacitor structure further includes a first plate between the dielectric layer and the insulating layer, and the semiconductor device further comprises a plug coupled to the first plate of the capacitor structure and to the first current carrying electrode of the transistor.

5. The semiconductor device of claim 4 wherein the first plate of the capacitor structure further includes:

a layer of titanium silicide overlying the plug for coupling the first plate to the plug;

a layer of titanium nitride overlying the layer of titanium silicide;

a layer of ruthenium overlying the layer of titanium silicide; and

a layer of ruthenium oxide overlying the layer of ruthenium.

6. A semiconductor device comprising:

a transistor having a current carrying electrode; and

a dielectric layer coupled to the current carrying electrode, wherein the dielectric layer is paraelectric and comprises tin.

7. The semiconductor device of claim 6 wherein the dielectric layer further comprises $Ba(Ti_{(1-x)}\ Sn_x)$, x having a value ranging between 0.1 to 0.3.

8. The semiconductor device of claim 6 further comprising:

an insulating layer overlying the transistor;

a first plate overlying the insulating layer;

a second plate overlying the first plate so that the dielectric layer is between the first plate and the second plate; and

a plug that couples the first plate to the current carrying electrode.

9. A dynamic random access memory comprising:

a transistor having a current carrying electrode; and

a dielectric layer coupled to the current carrying electrode, wherein the dielectric layer is paraelectric and comprises tin.

10. A semiconductor device having a capacitor, wherein the capacitor comprises:

a first plate of conductive material;

a second plate of conductive material; and

a layer of dielectric material between the first plate of conductive material and the second plate of conductive material, wherein the layer of dielectric material comprises $Ba(Ti_{(1-x)}\ Sn_x)O_3$ in solid solution form.

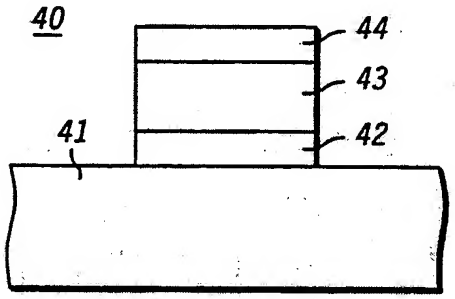


FIG. 1A

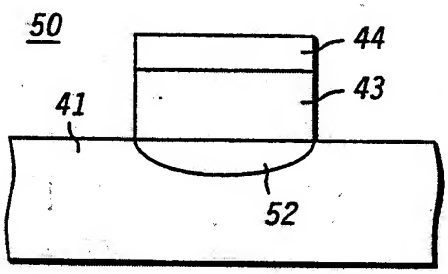


FIG. 1B

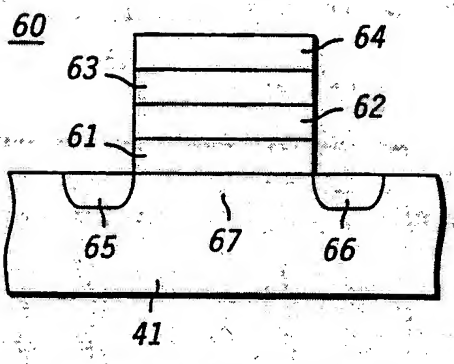


FIG. 1C

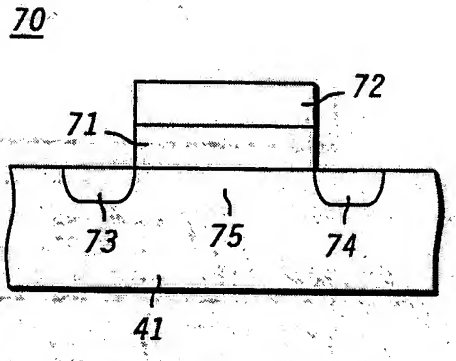


FIG. 1D

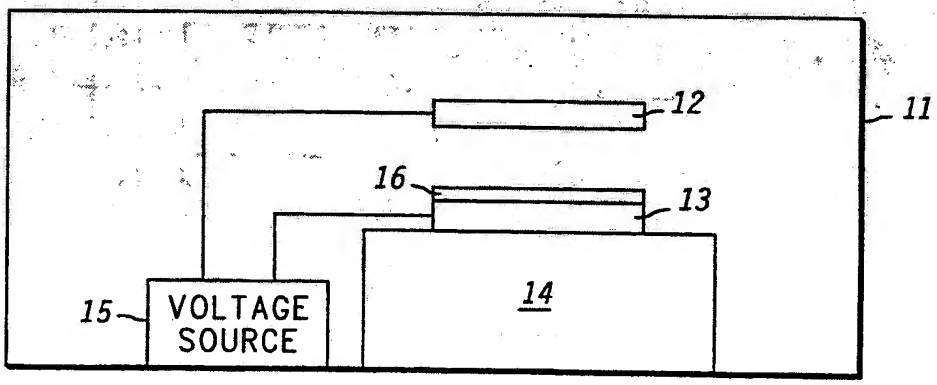


FIG. 2

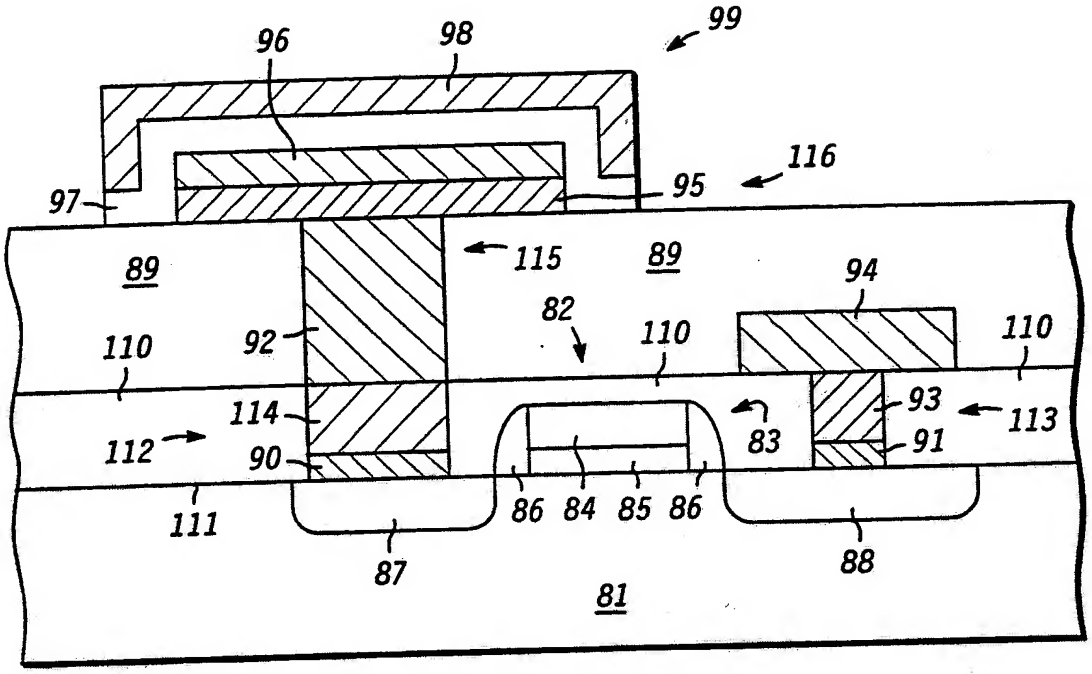
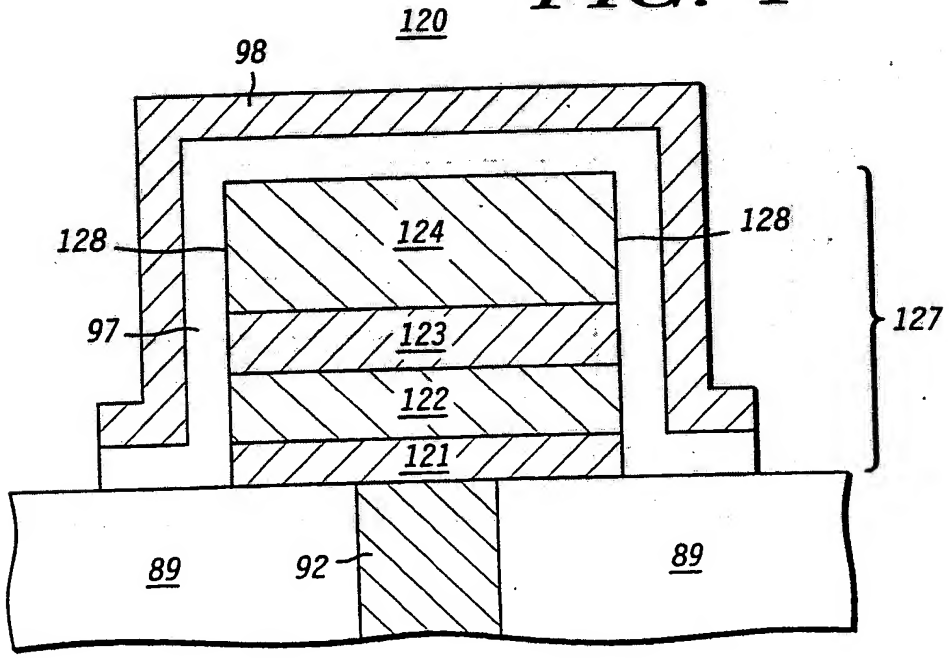


FIG. 3

FIG. 4



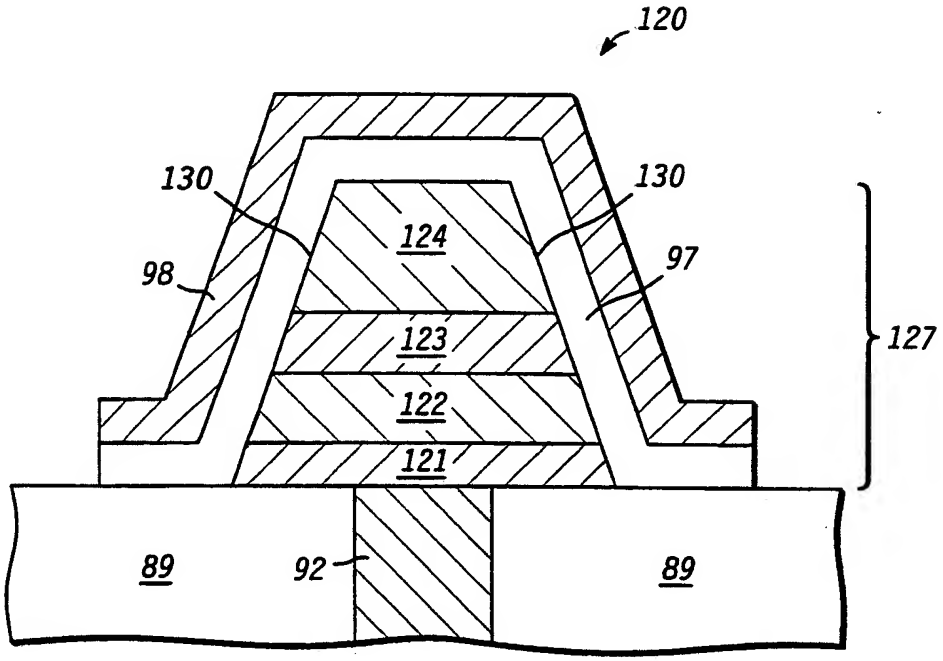

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FIG. 5

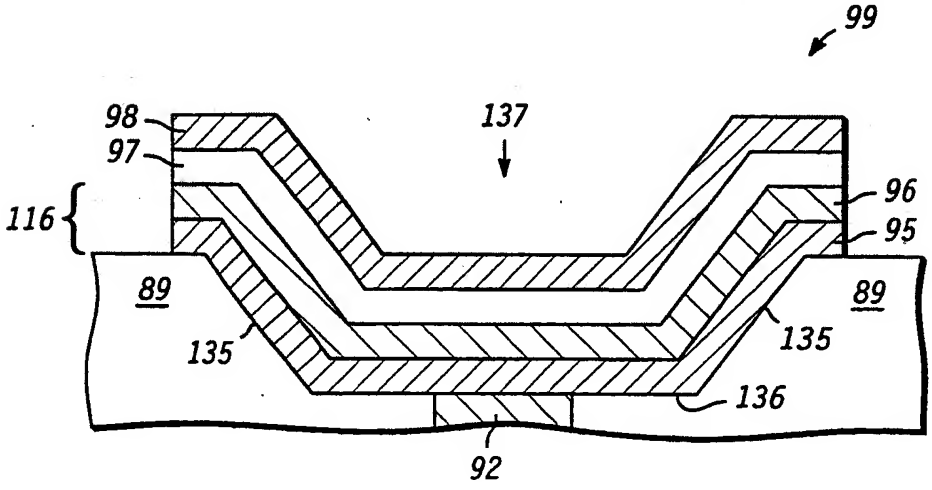
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FIG. 6

INTERNATIONAL SEARCH REPORT

I. ...national Application No
PCT/US 98/05634

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L27/108 H01L27/115 H01L21/3205

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	US 5 499 207 A (MIKI HIROSHI ET AL) 12 March 1996 see column 4, line 55 - column 7, line 47; figures 1,5-8	1,4,6, 8-10 5 2,3
Y	US 5 605 858 A (NISHIOKA YASUSHIRO ET AL) 25 February 1997 see column 5, line 42 - column 6, line 65; figures 1-7; table 1	5
X A	WO 96 02067 A (SYMETRIX CORP ;MATSUSHITA ELECTRONICS CORP (JP)) 25 January 1996 see page 4, line 20 - page 5, line 25; figure 1 see page 12, line 29 - page 13, line 6; figure 11	1-3,6,7, 9,10

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
7 July 1998	16/07/1998

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 98/05634

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 343 353 A (MIKI HIROSHI ET AL) 30 August 1994	1,4,6, 8-10
A	see column 7, line 11 - column 8, line 68; figures 5-10	2,3,5,7

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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Docket # MUH-12757

Applic. #_____

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